WHAT IS CLAIMED IS:

1. A method of computer aided design comprising:

providing a description of a first logic function using a high-level design language;

synthesizing gates to obtain a first alternative netlist for the first logic function;

performing a technology mapping of the first alternative netlist to obtain a first mapping netlist;

synthesizing gates to obtain a second alternative netlist for the first logic function;

performing a technology mapping of the second alternative netlist to obtain a second mapping netlist;

selecting one of corresponding first mapping netlist or second mapping netlist based on a comparison of the first mapping netlist with the second mapping netlist based on design criteria, wherein the selected one of the corresponding first mapping netlist or second mapping netlist is a selected mapping netlist;

optimizing the selected mapping netlist; and

performing a technology mapping on the second mapping netlist after optimizing.

2. The method of claim 1 wherein the design criteria includes optimizing for area.

3. The method of claim 1 wherein the design criteria includes optimizing for delay.

4. The method of claim 1 wherein the first mapping netlist comprises look-up table structures.

5. The method of claim 1 wherein the first mapping netlist comprises digital signal processing blocks.

6. The method of claim 1 wherein the first alternative netlist comprises logic gates.

7. The method of claim 1 wherein the step of performing a technology mapping of the first alternative netlist to obtain a first mapping netlist is done a copy of the first alternative netlist.

8. A method comprising:

generating a first alternative netlist for a logic function;

generating a second alternative netlist for the logic function, wherein the second alternative netlist has a different gate configuration from the first alternative netlist; and

selecting one of the first or second alternative netlists as a selected alternative netlist based on results of a technology mapping of the first and second alternative netlists.

9. The method of claim 8 further comprising:

performing a synthesis optimization on the selected alternative netlist to obtain an optimized selected alternative netlist.

10. The method of claim 8 further comprising:

performing a synthesis optimization on the selected alternative netlist to obtain an optimized selected alternative netlist; and

performing a technology mapping on the optimized selected alternative netlist.

11. The method of claim 8 wherein the selecting one of the first or second alternative netlists is based on area.

12. The method of claim 8 wherein the selecting one of the first or second alternative netlists is based on depth.

13. A method comprising:

generating a netlist for a logic function;

performing a first technology mapping on the netlist;

after the first technology mapping, performing a synthesis optimization on the netlist; and

after the synthesis optimization, performing a second technology mapping on the netlist.

14. The method of claim 13 wherein the first technology mapping maps the netlist to the same target technology as the second technology mapping.

15. The method of claim 13 wherein the logic function is provided in a high-level design language.